

FIG. 1

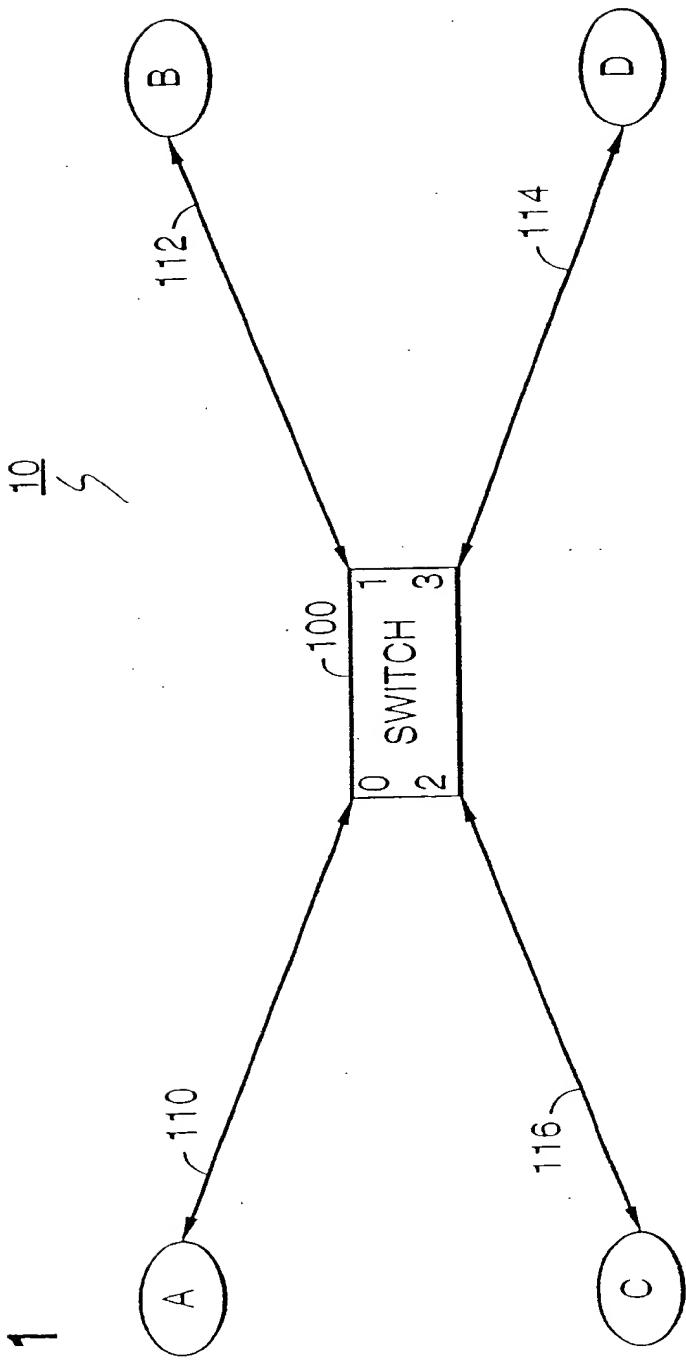


FIG. 3A

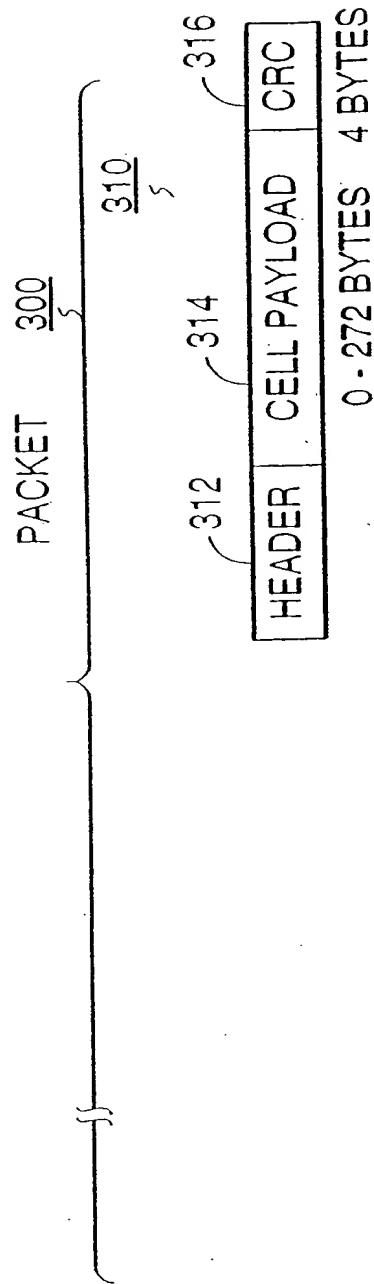
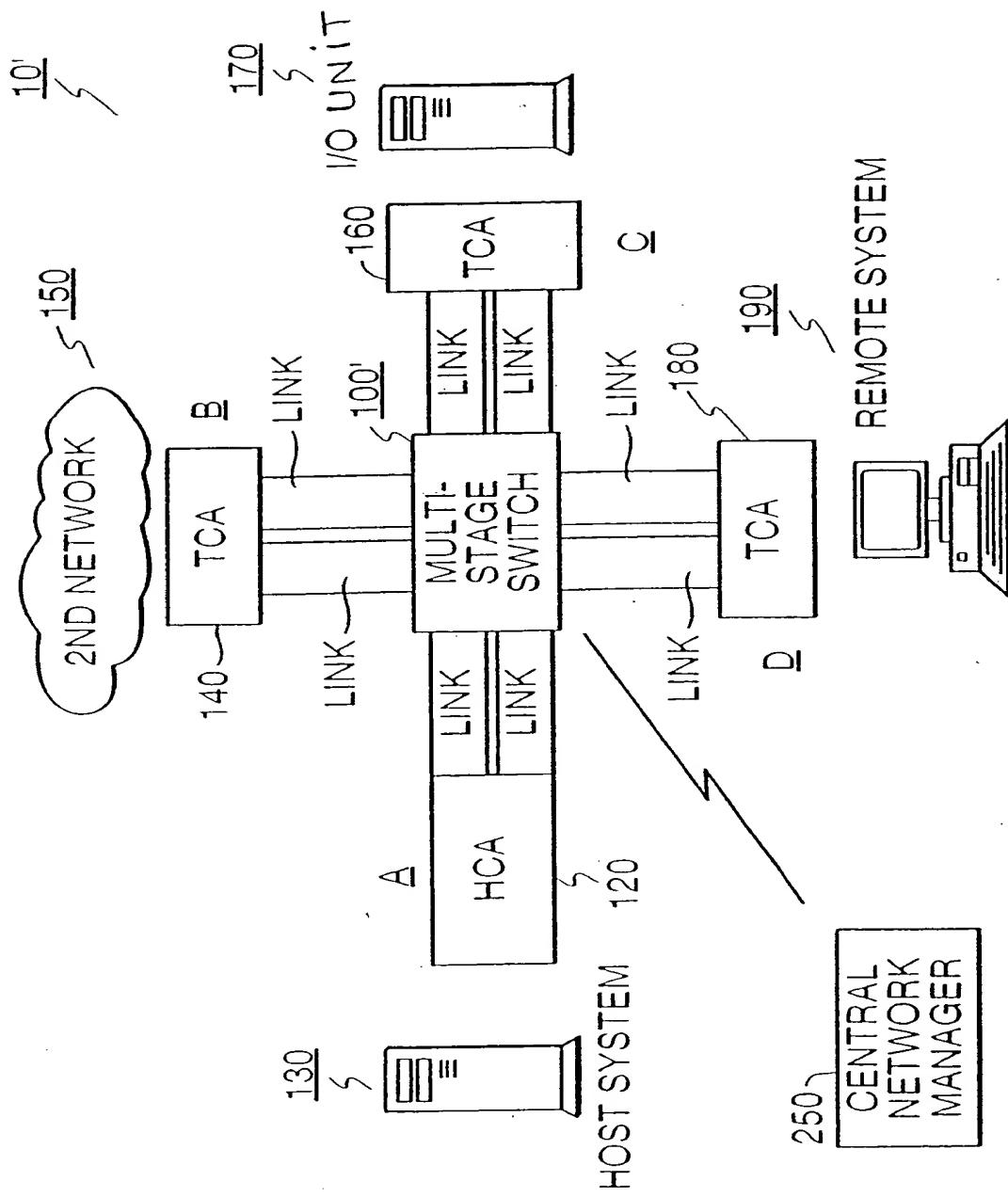


FIG. 2



350A

↙

↙
360

| CONTROL SEGMENT | | |
|-----------------|---------------|-----------------|
| LENGTH | MEMORY HANDLE | VIRTUAL ADDRESS |
| 372 | 374 | 376 |

370

FIG. 3B

350B

↙

↙
360

| CONTROL SEGMENT | | |
|-----------------|-------------------------|---------------------------|
| | REMOTE MEMORY HANDLE | REMOTE VIRTUAL ADDRESS |
| 372 | 382 | 384 |
| 372 | 374 | 376 |

380

370

FIG. 3C

FIG. 4A

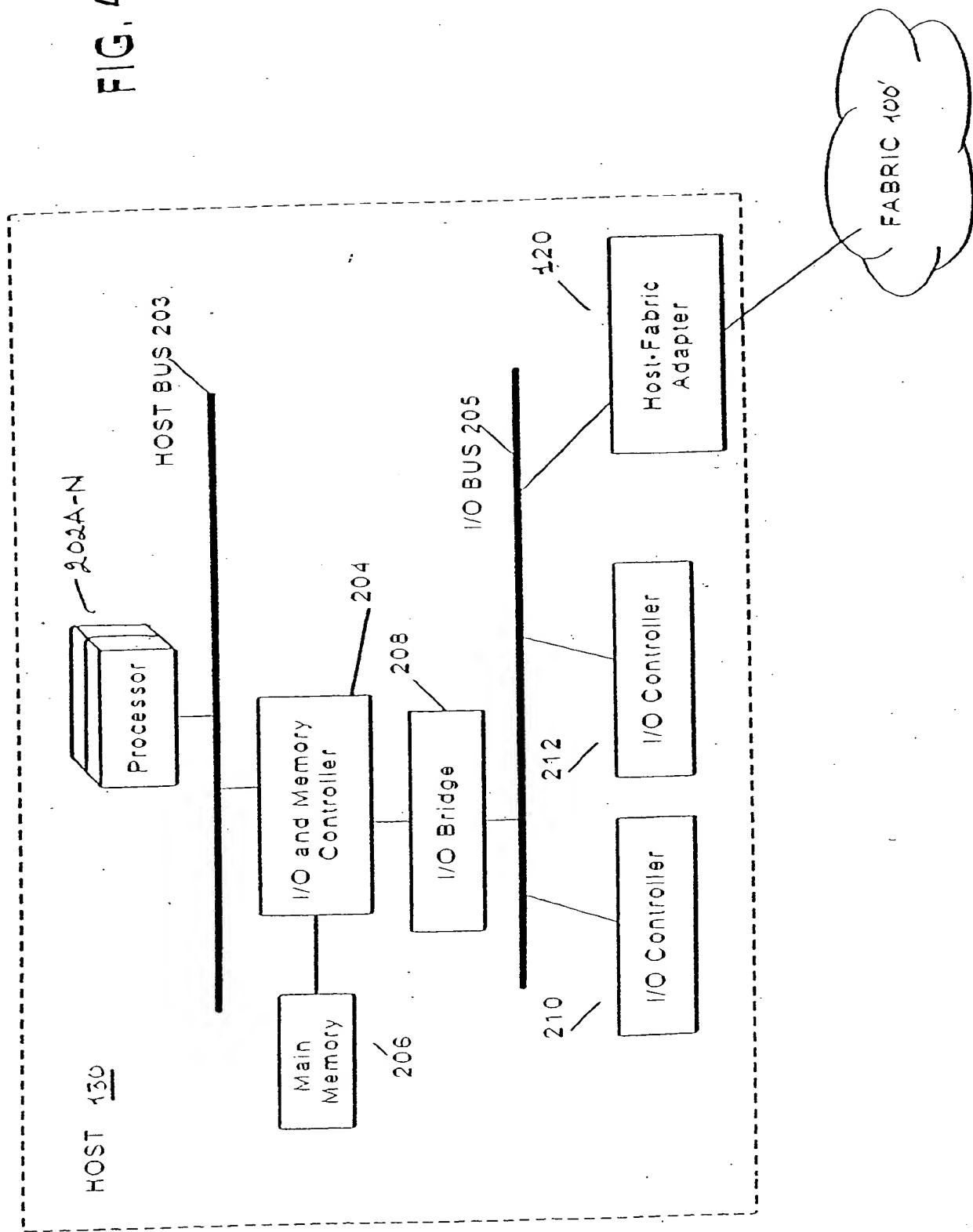
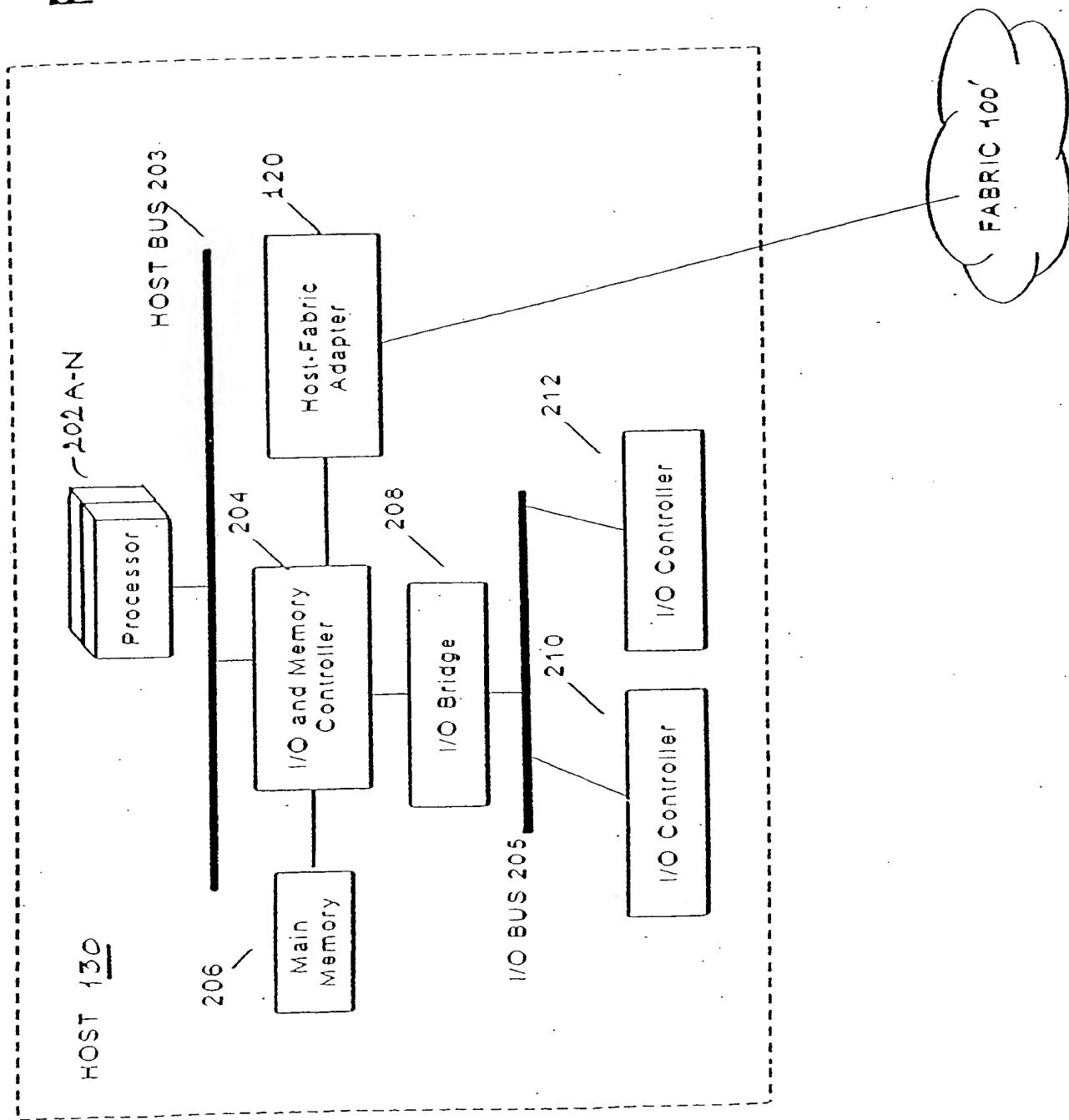
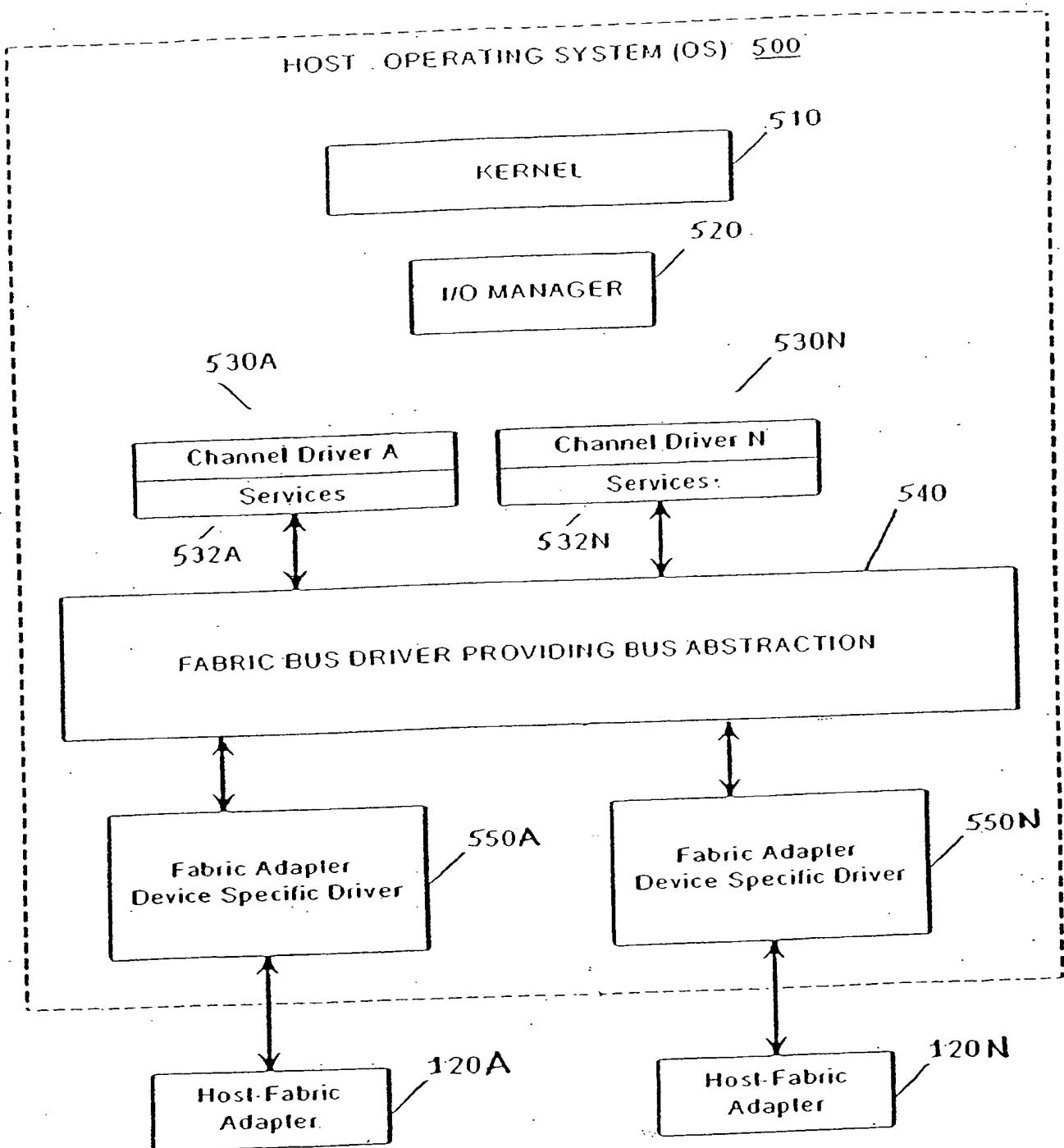


FIG. 4B





EXAMPLE SOFTWARE DRIVER STACKS OF HOST SYSTEM

FIG. 5

FIG. 6

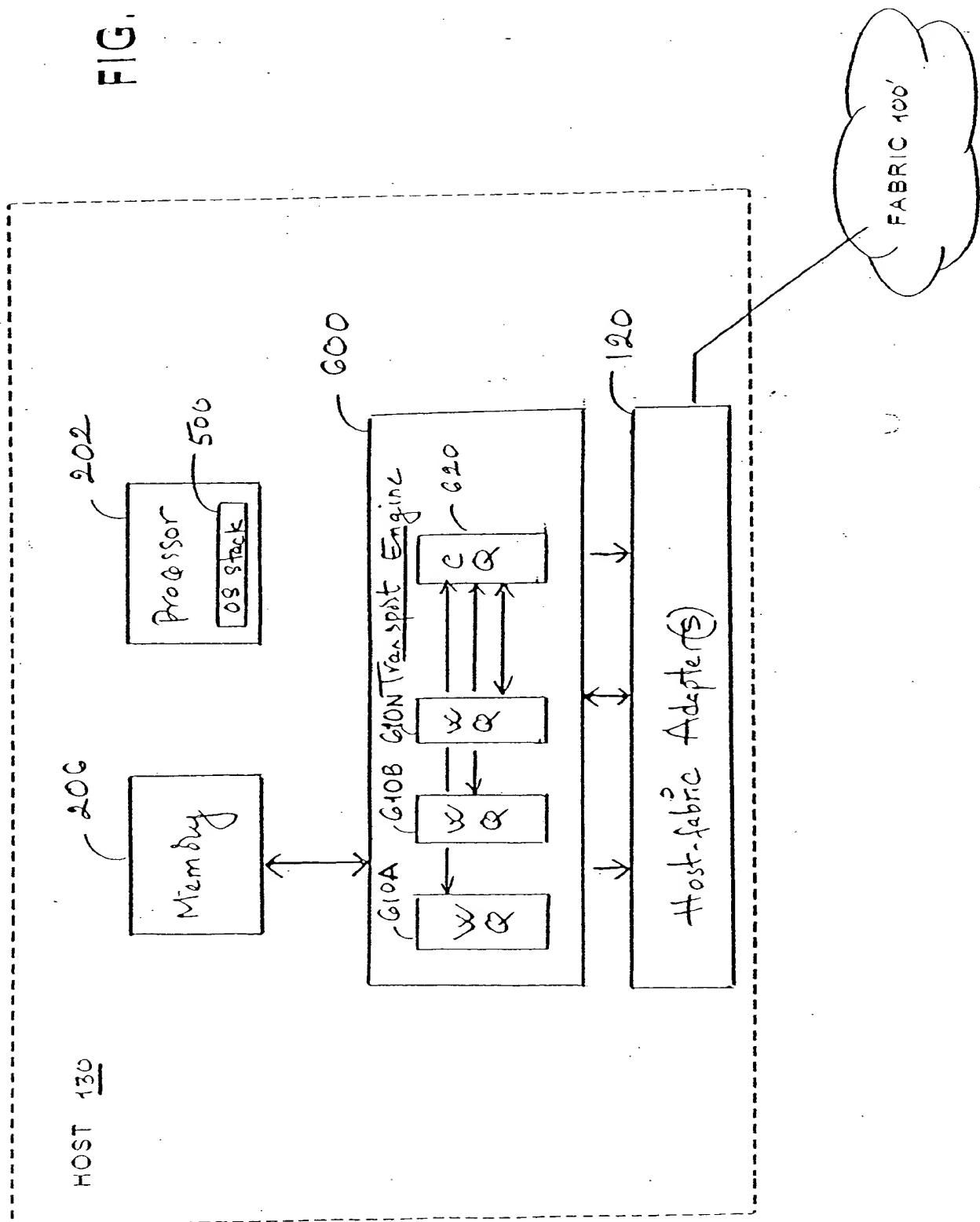
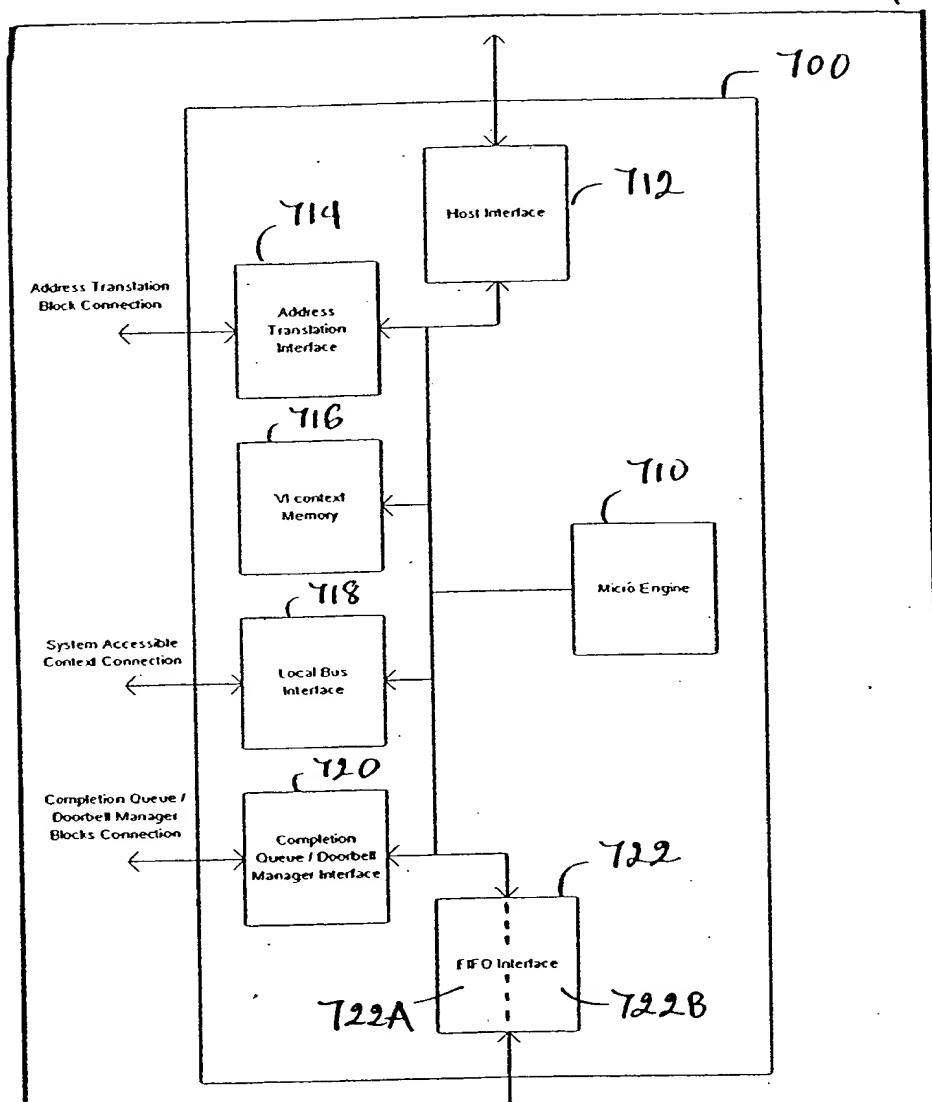


FIG. 7

120

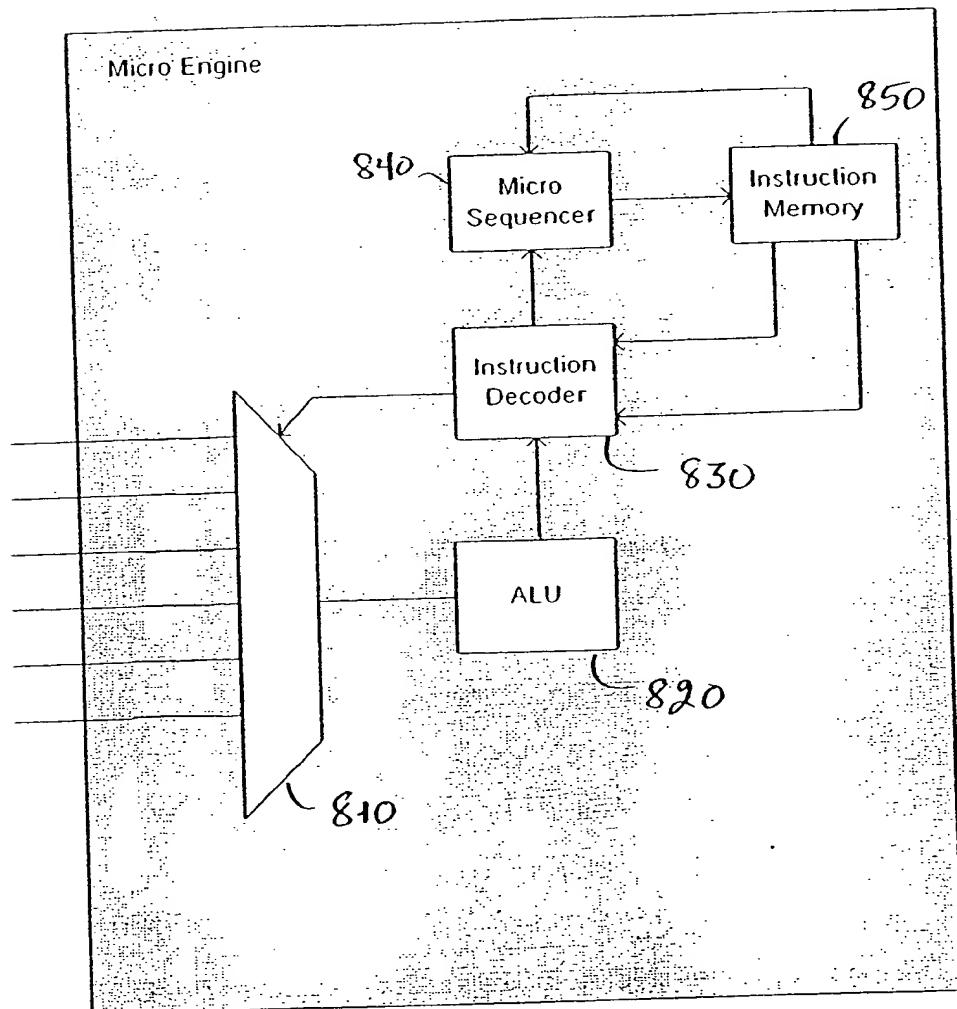


Solid Interface

FABRIC 100'

FIG. 8

710
5



710
3
FIG 9 ~~Diagram of the CPU~~

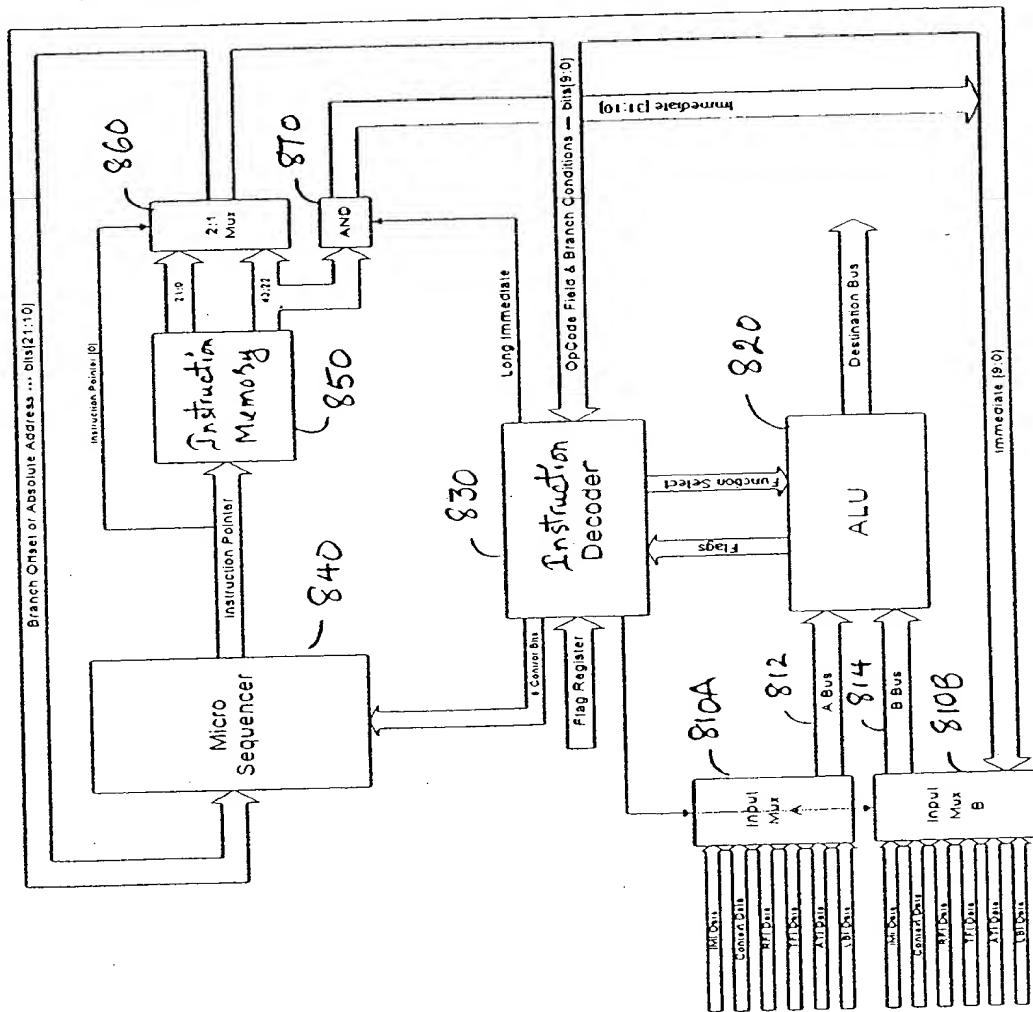
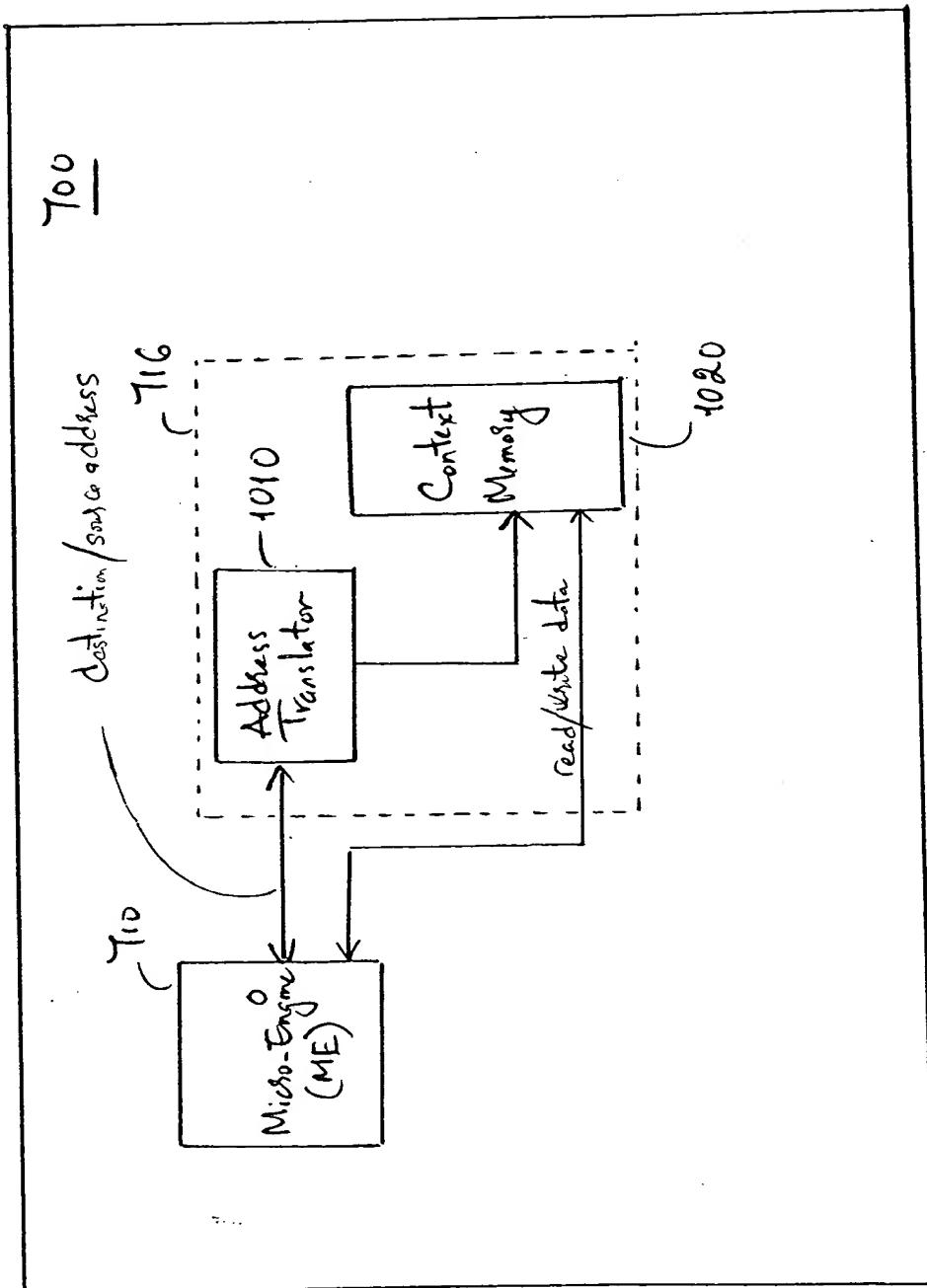


FIG. 10



Single Memory
40x32

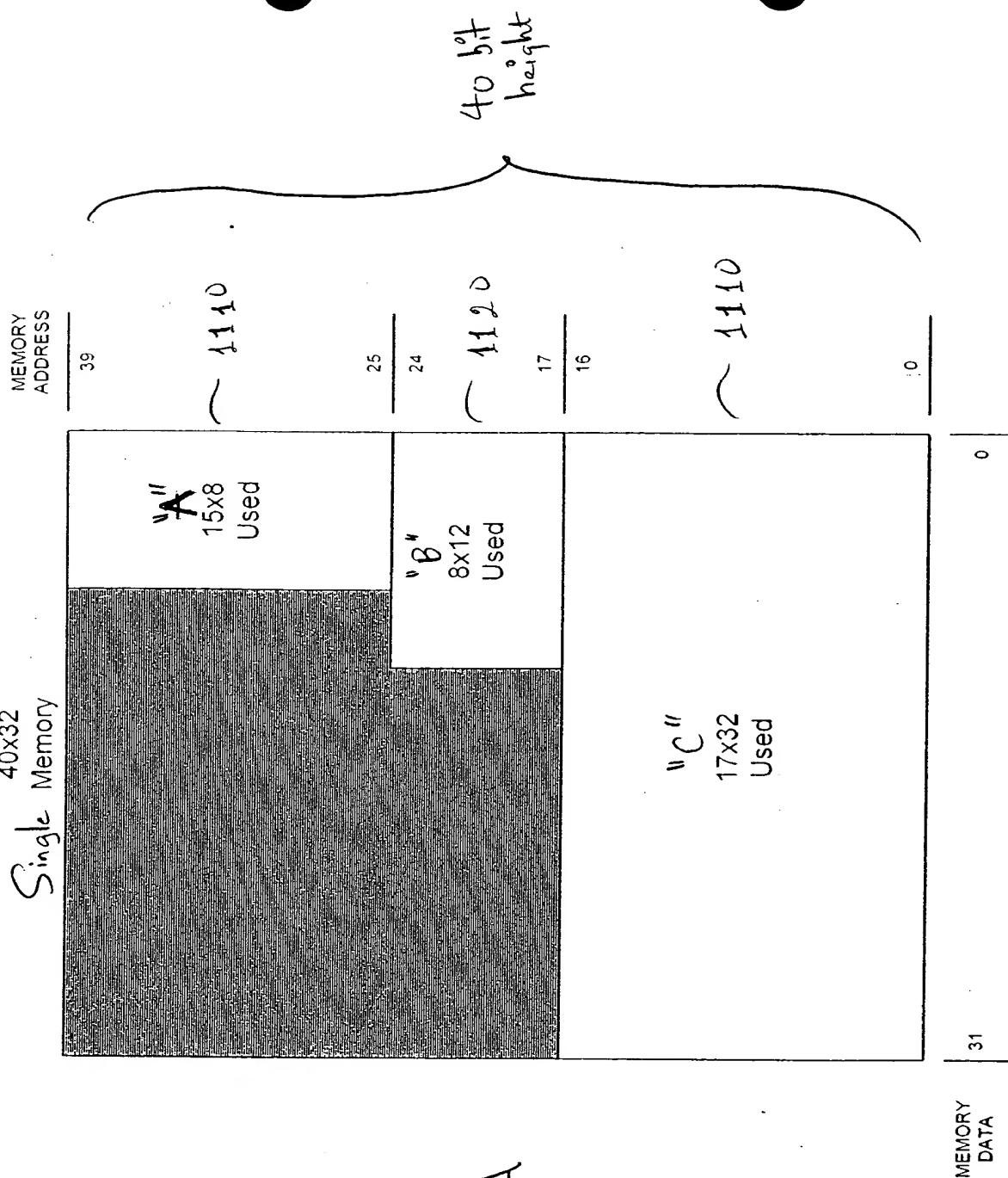
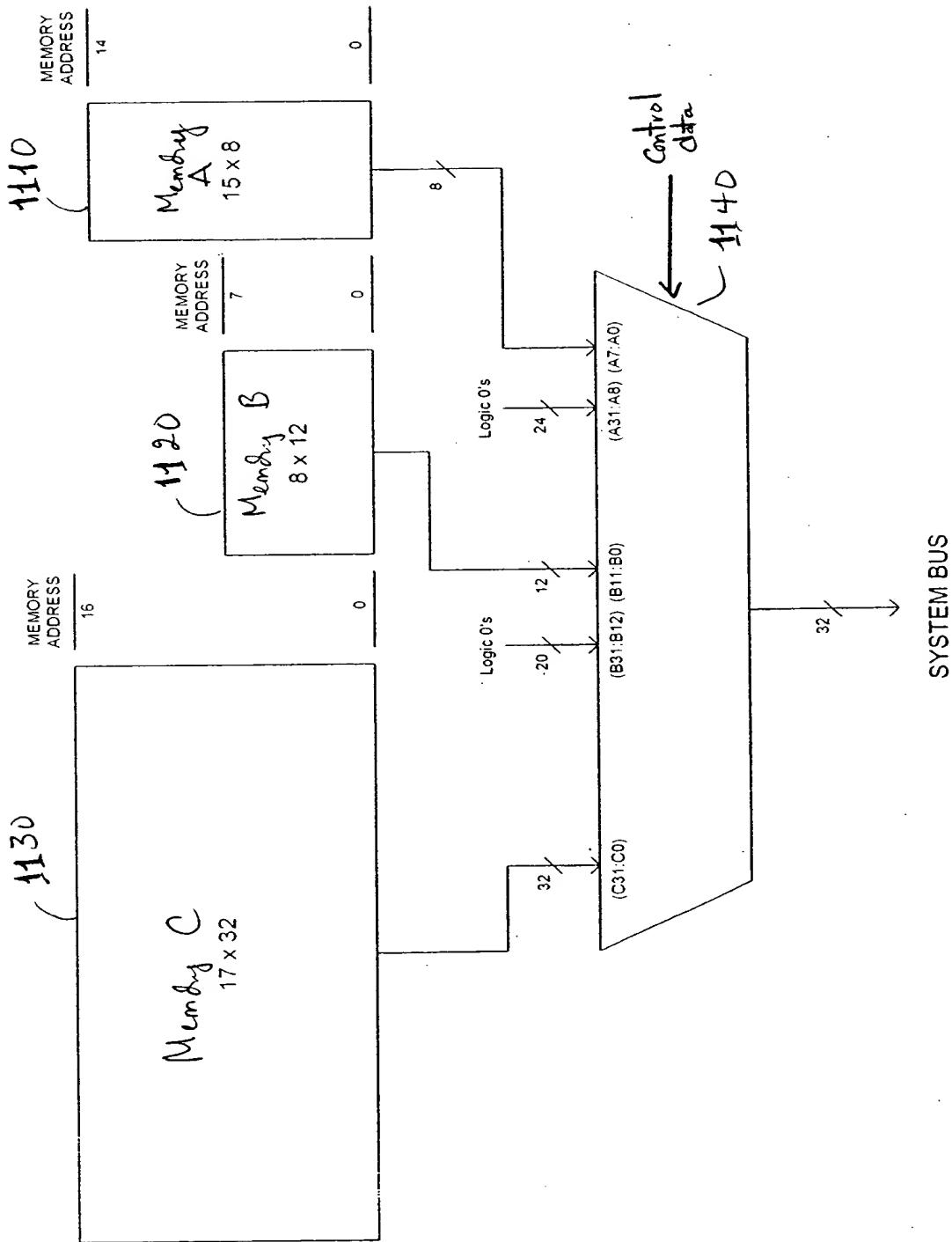


FIG. 11A

FIG. 11B



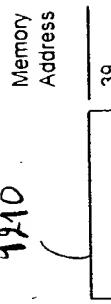
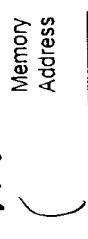
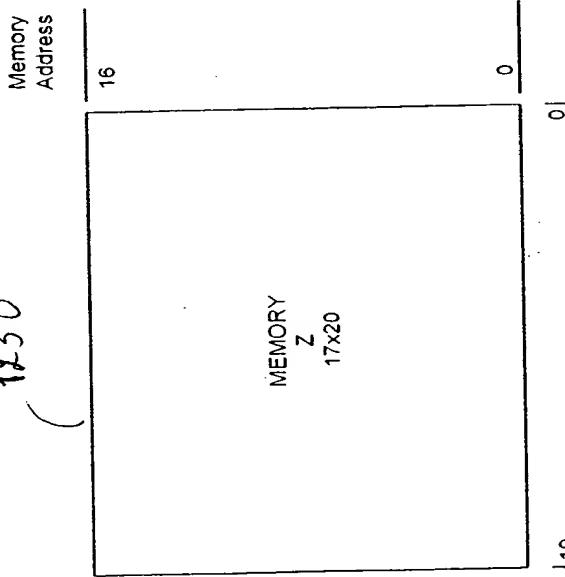


FIG. 12A

1220



1230



Memory Data
19

Micro-Engine Data
31

DATA STRUCTURE

1910

Memory Address

$n = 39$

1910

1920

1920
Memory Address

| | |
|------|----------------|
| "0S" | $(m + 1) = 25$ |
| | $m = 24$ |

MEMORY
A
 40×8

1930
Memory Address

| | |
|------|----------------|
| "0S" | $(l + 1) = 17$ |
| | $l = 16$ |

MEMORY
B
 25×4

1930
Memory Address

| | |
|------|----------------|
| "0S" | $(l + 1) = 17$ |
| | $l = 16$ |

MEMORY
Z
 17×20

Memory Data
19

Micro-Engine
Data
31

0

0

0

0

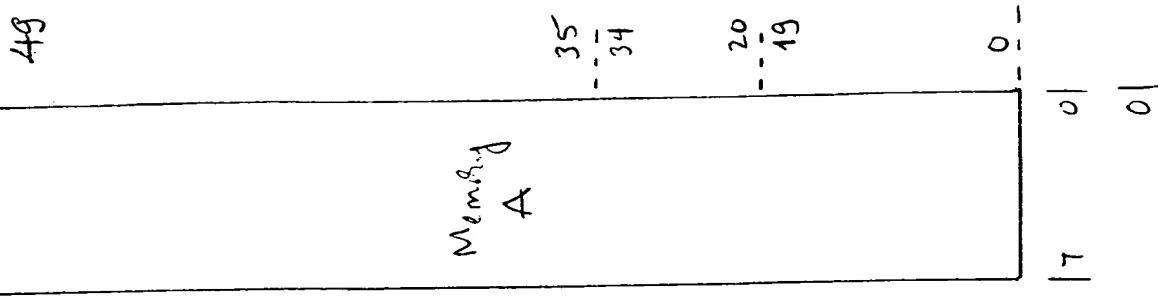
0

0

0

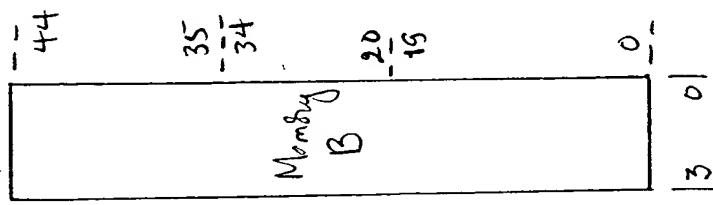
0

1340



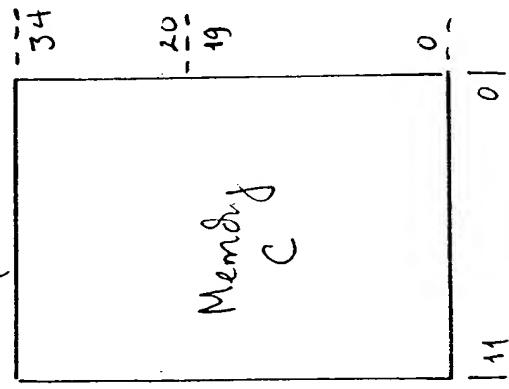
49

1320



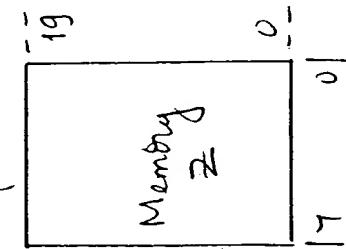
44

1330



34

1340



19

FIG. 13A

Memory data

Micro Engine 131
data2

1310

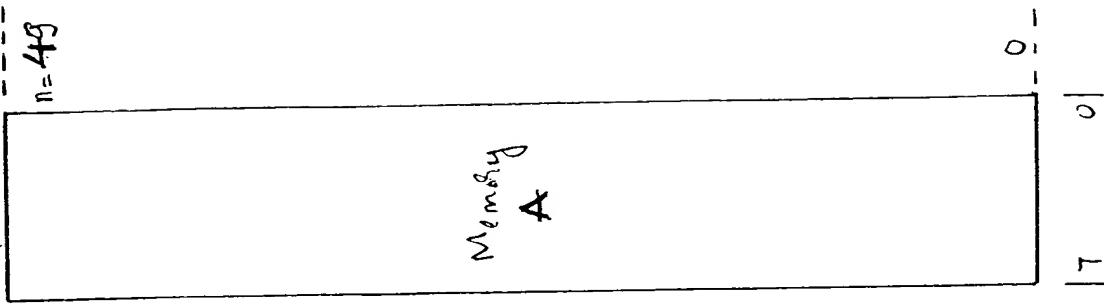
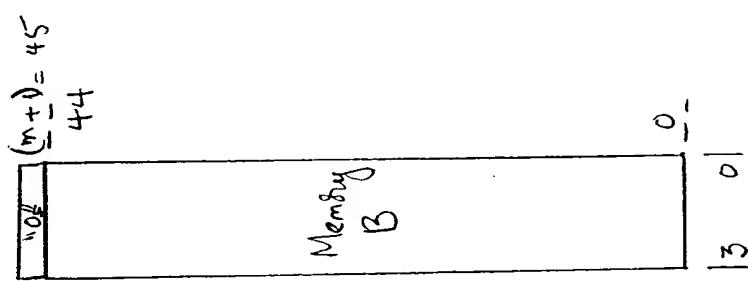
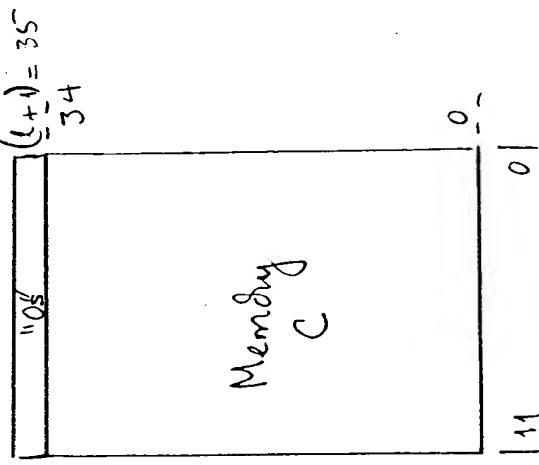


FIG. 13B

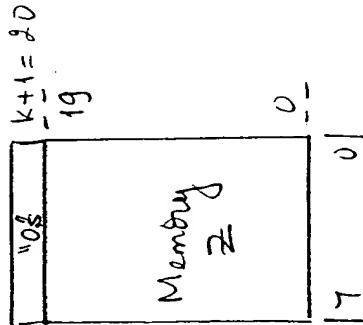
1320



1330



1340

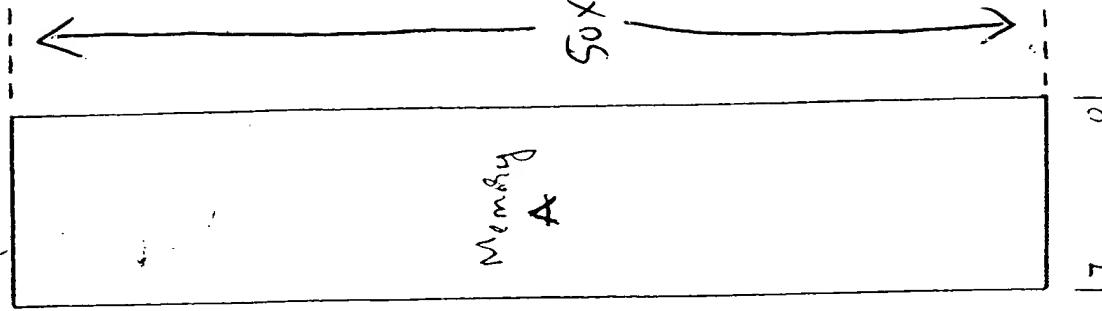


Memory data

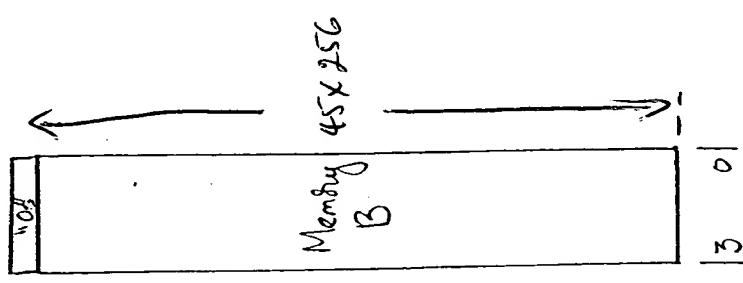
Microtronic 131
data

01

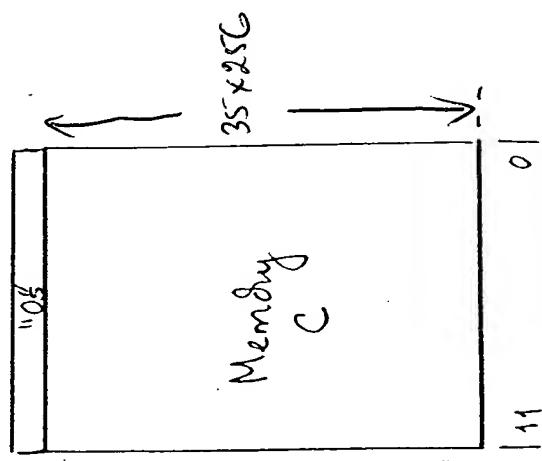
୧୪୧୦



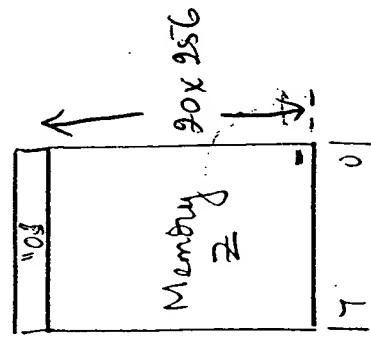
୧୪୨୦



୧୪୩୦



୧୪୪୦



Memory
data

Microengine
data

0 |

1 |

1 |

3 | 0 |

0 |

1 |

0 |

1 |

0 |